J1050 U.S. PTO
10/092310
03/07/02

PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10092310	03/07/2002	430	271.1	1752	WILSON

**APPLICANTS: Otoguro Akihiko; Takechi Satoshi;

**CONTINUING DATA VERIFIED: None Acu

** FOREIGN APPLICATIONS VERIFIED: None
JAPAN 2001-180584 06/14/2001

PG-PUB DO NOT PUBLISH ☐ RESCIND ☐

Foreign priority claimed ☑ yes ☐ no
35 USC 119 conditions met ☑ yes ☐ no
Verified and Acknowledged Examiner's Initials John C Wilson

ATTORNEY DOCKET NO
020201

TITLE : Multi-layered resist structure and manufacturing method of semiconductor device

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAMER	PREPARED FOR ISSUE	Application Examiner

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)